In the Specification

Please amend paragraph **[0001]** *as follows:*

This case is related to United States Patent Application Serial Nos. 10/813,907 and 10/814,868 filed on even date herewith, in the name of the same inventors, bearing the same title and commonly assigned herewith. (Attorney Docket Nos. IMPJ-0027A and IMPJ-0027C).

This case is also related to United States Patent Application Serial No. 10/814,867, entitled "High-Voltage Switches in Single-Well CMOS Processes", filed on even date herewith in the name of inventors Frederic Bernard, Christopher J. Diorio, Troy N. Gilliland, Alberto Pasavento, Kaila Raby, Terry D. Hass and John Hyde and commonly assigned herewith. (Attorney Docket No. IMPJ-0031).

Please amend paragraph **[0017]** *as follows:*

Referring first to FIG. 3, there is shown a block diagram of a rewriteable electronic fuse 30, according to an embodiment of the present invention. The rewriteable electronic fuse 30 is used in conjunction with logic (LOGIC) and comprises a latch (or logic gate(s)) 32 coupled to a rewriteable nonvolatile memory element 34. During operation, the latch or logic gate(s) 32 is coupled to a reset signal, $\overline{\text{RESET}}$, or to a power supply source, Vdd. As explained in more detail below, the nonvolatile memory element 34 is configured so that it may be programmed to a memory value capable of causing the latch or logic gate 32 to settle to a predetermined state as a power-up or a reset signal is applied to the fuse 30, i.e., as Vdd or $\overline{\text{RESET}}$ is applied to the fuse 30.

Please amend paragraph **[0037]** *as follows:*

FIG. 13 shows a master-slave rewriteable electronic fuse 128, according to an embodiment of the present invention. The master-slave rewriteable electronic fuse 128 is used with logic (LOGIC) and comprises a master fuse 130 coupled to a slave latch 132. The master fuse 130 comprises a rewriteable electronic fuse, e.g., any one of the types described above, and is controlled by a master signal, (shown in FIG. 13 as RESET), applied to a master terminal of

the master fuse 130. The slave latch 132 is controlled by a slave-latch signal (shown in FIG. 13 as $\overline{\text{RESET}}$), applied to the slave-latch terminal of the slave latch 132. Application of RESET causes the master fuse 130 to settle to a predetermined state as described above. After the master fuse 130 has settled to its predetermined state, $\overline{\text{RESET}}$ is applied to the slave-latch terminal of the slave latch 132 to latch and hold the state of the master fuse 130.

Please amend paragraph **[0020]** *as follows:*

As shown in FIG. 4, a first rewriteable nonvolatile memory element 48 is coupled to the first output terminal, OutBar, of the rewriteable electronic fuse 40, and a second rewriteable nonvolatile memory element 50 is coupled to the second and complementary output terminal, Out, of the fuse 40. More specifically, a drain (D) of the first nonvolatile memory element 48 is coupled to the first output terminal, OutBar, and the drain (D) of the second nonvolatile memory element 50 is coupled to the second output terminal, Out. The sources(S) of the first and second nonvolatile memory elements 48, 50 are both coupled to a power supply (or reset signal) input terminal (here illustrated as Vdd). First rewriteable nonvolatile memory element 48 has a floating gate fg0. Second rewriteable nonvolatile memory element 50 has a floating gate fg1. Because a nonvolatile memory element is coupled to each "side" of the half-latch, i.e., to both the OutBar and Out terminals, and because each nonvolatile memory element is coupled in series between the half-latch and the power-supply voltage (or reset) terminal, this embodiment of the present invention is referred to as a "symmetrical serial half-latch fuse".

Please amend paragraph **[0023]** *as follows:*

According to an aspect of the present invention, the nonvolatile memory elements in the various embodiments of the invention described in this disclosure may comprise floating-gate transistors. The amount of charge stored on the floating gate of a given floating-gate transistor determines the memory value provided and, consequently, the state to which the latch latches. FIG. 5A shows a floating-gate pFET 52, which may be used to form the first and/or second nonvolatile memory elements 48 and 50 in FIG. 4 and other nonvolatile memory elements in other embodiments of the invention. The floating-gate pFET 52 is formed in an n- well disposed in a p- substrate. A p+ source and p+ drain are formed in the n- well. The floating gate pFET

includes a floating gate (fg) 54 disposed over a thin dielectric layer 56. Electrons may be added to and removed from the floating gate 54 by various mechanisms including Fowler-Nordheim (FN) tunneling, impact-ionized hot-electron injection (IHEI), direct (bi directional) tunneling (if the dielectric layer is thin enough), hot-hole injection, band-to-band tunneling induced hot-electron injection, ultraviolet radiation exposure, or a variety of other means as are well known to those practiced in the art. These charging mechanisms allow the various fuse embodiments of the present invention to be "rewriteable ". Some of the various mechanisms for programming memory elements implemented using floating-gate transistors are described in more detail below.

Please amend paragraph **[0024]** *as follows:*

FIG. 5B shows an alternative floating-gate pFET 58, which may be used to form the nonvolatile memory elements of the various fuse embodiments of the present invention. Similar to the floating-gate transistor 52 in FIG. 5A, the floating-gate transistor 58 in FIG. 5B has a single conductive layer used to form the floating gate 60 of the device. It comprises a storage transistor formed from an n- well disposed in a p- substrate, with a p+ gate and a p+ drain formed in the n- well. An additional control implant 62 (which may be p+ or n+) is included in the floating-gate transistor 58 in FIG. 5B to provide a control-gate terminal. The storage transistor and control implant 62 share floating gate 60, which is a common floating gate. This type of floating-gate transistor 58 and how it may be programmed is described in U.S. Patent No. 5,761,121.

Please amend paragraph **[0025]** *as follows:*

The floating-gate transistors 52 and 58 shown in FIGS. 5A and 5B are beneficial in that they use a single conductive gate layer (typically polysilicon). This single-layer architecture makes these types of nonvolatile memory elements and, consequently, the fuses within which they are embedded, amenable to fabrication in standard, single-poly CMOS (Complementary Metal Oxide Semiconductor) semiconductor fabrication processes. The nFETs 53 and 59 as shown in FIGS. 5C and 5D may also be utilized to realize CMOS compatible nonvolatile memory elements. In FIG. 5C, a storage transistor is formed of an n+ source region and an n+ drain region formed in a p- substrate, with a floating gate 54 provided over the channel disposed

between the source and drain. In FIG. 5D, the floating gate transistor 59 comprised of a storage transistor formed of n+ source region and n+ drain region disposed in a p- substrate includes an additional control gate implant 62 (which may be p+ or n+) which shares floating gate 60 with the storage transistor. Other types of floating-gate transistors may also be used to form the nonvolatile memory elements of the various fuse embodiments of the present invention. For example, FIGS. 5E and 5F show p-type and n-type floating-gate transistors 64 and 66, respectively, fabricated in a double-poly process. The floating gate 68 of each floating-gate transistor is formed in a first polysilicon layer, and a control gate 70 is formed in a second polysilicon layer. Other components of these transistors include, for the pFET, an n- well provided in a p- substrate, with a p+ drain and a p+ source formed in the n- well, and for the nFET, an n+ drain and an n+ source provided in a p- substrate. In accordance with alternative embodiments of the present invention, the double-poly floating-gate transistors shown in FIGS. 5E and 5F may be used to form the nonvolatile memory elements of the various fuse embodiments of the present invention.

Please amend paragraph **[0027]** *as follows:*

Referring now to FIG. 7, there is shown a rewriteable electronic fuse 72, according to an embodiment of the present invention. This "self-latching symmetric serial fuse" 72 comprises two cross-coupled CMOS inverters (the output of a first inverter connected to the input of a second inverter and the output of the second inverter connected to input of the first inverter) 74 and 76, and two nonvolatile memory elements 78 and 80. A first nonvolatile memory element 78 of the two nonvolatile memory elements 78 and 80 includes a floating gate fg0 and is coupled in series between a first 74 of the two inverters 74 and 76 and a power supply (or reset signal) input terminal, and the second nonvolatile memory element 80 includes a floating gate fg1 and is coupled in series between a second 76 of the two inverters 74 and 76 and the power supply (or reset signal) input terminal. Together the two cross-coupled inverters 74 and 76 form a full-latch 82, comprised of half-latches latch_1 and latch_0. Similar to the presence of the first and second nonvolatile memory elements 48, 50 in the symmetrical serial half-latch fuse 40 in FIG. 4, the first and second nonvolatile memory elements 78, 80 in the self-latching symmetric serial fuse 72 in FIG. 7 cause the latch 82 to settle to a predetermined state during a power-up or reset of the

fuse 72. The state to which the latch 82 settles is determined by the memory values stored on the nonvolatile memory elements 78, 80.

Please amend paragraph **[0029]** *as follows:*

FIG. 8 shows a rewriteable electronic fuse 84, according to an embodiment of the present invention. This "self-latching symmetric parallel fuse" 84 comprises two cross-coupled CMOS inverters 86 and 88, and two nonvolatile memory elements 90 and 92. Together the two cross-coupled inverters 86, 88 form a full-latch 89 comprised of half-latch latch 0 and half-latch latch 1. In accordance with this embodiment, a first 90 of the two nonvolatile memory elements 90, 92 includes a floating gate fg0 and is coupled in parallel with a transistor of a first one 86 of the two inverters 86, 88, and the second 92 of the two nonvolatile memory elements 90, 92 includes a floating gate fg1 and is coupled in parallel with a transistor of the second 88 of the two inverters 86, 88. Similar to the embodiments described above, and to those in other parts of this disclosure, the first and second nonvolatile memory elements 86, 88 in the self-latching symmetric parallel fuse 84 in FIG. 8 cause the latch 89 to settle to a predetermined state during a power-up or reset of the fuse 84. For example, assume that floating-gate transistors are used for the first and second nonvolatile memory elements 90, 92, and suppose the floating-gate voltage on the first nonvolatile memory element 90 (i.e. Vfg0) has been previously programmed to Vdd and that the floating-gate voltage on the second memory element (i.e. Vfg1) 92 has been previously programmed to Gnd. With Vfg0 = Vdd, the first nonvolatile memory element 90 remains OFF. When Vdd (or a reset signal) is applied to the fuse 84, the second nonvolatile memory element 92 turns ON and the Out terminal is pulled down to Gnd. When Out is at Gnd, the latch will settle with OutBar at Vdd. Hence, the fuse 84 settles to the state: OutBar = Vdd and Out = Gnd. To program the fuse 84 to the complementary state, the memory values of the first and second nonvolatile memory elements would be reversed. For example, if floating-gate transistors are used to implement the nonvolatile memory elements 90, 92, the relative amount of charge stored on the floating gates of the memory elements would be modified so that Vfg0 is near or below Gnd, and Vfg1 is near or above Vdd. Finally, if the floating-gate transistors 90, 92 were constructed from nFETs rather than from pFETs, the logical polarities would be reversed

(i.e. storing Vfg0 = Gnd and Vfg1 = Vdd would cause the latch to latch with Out = Gnd and OutBar = Vdd).

Please amend paragraph **[0030]** *as follows:*

FIG. 9 shows a rewriteable electronic fuse 94, according to an embodiment of the present invention. This "self-latching asymmetric serial fuse" 94 comprises two cross-coupled CMOS inverters 96 and 98 and a nonvolatile memory element 100 coupled in series between a first 96 of the two inverters 96, 98 and a power supply (or reset) input terminal. The two cross-coupled CMOS inverters 96 and 98 include a first half-latch latch_0 and second half-latch latch_1. So long as fg1 in the single nonvolatile memory element 100 is set near or above Vdd, pFET 100 will be turned off, and inverter 96 will not have a conduction path to Vdd (or to reset, as appropriate). Consequently, the latch will settle with Out = Gnd and OutBar = Vdd. If, however, fg1 is set well below Vdd, such that pFET 100 is turned on, the state to which the latch latches is not necessarily deterministic. To make the latching more deterministic, the gate width-to-length ratio of a pFET (or nFET, or both) of one of the two inverters 96, 98 can be adjusted so that the difference in transistor sizes beneficially disrupts the symmetry of the asymmetric latch when the nonvolatile memory element 100 is off, thereby influencing the fuse to latch deterministically with Out = Vdd and OutBar = Gnd. Other mechanisms for disrupting the symmetry of the latch will now be apparent to those of ordinary skill in the art. For example, the channel doping of the various transistors in the latch may be individually selected to achieve the same result, the relative channel doping reflecting the impedance of the transistor much the same way as the relative gate widths. Also, placing one or two capacitors between one or two latches outputs and a fixed voltage source such as Vdd or Gnd can achieve the same effect as discussed below, e.g., in connection with the discussion of FIG. 11. Other mechanisms for achieving the same result will now be readily apparent to those of ordinary skill in the art.

Please amend paragraph **[0031]** *as follows:*

FIG. 10 shows a rewriteable electronic fuse 102, according to an embodiment of the present invention. This "self-latching asymmetric parallel fuse" 102 comprises two cross-coupled CMOS inverters 104 and 106 and a nonvolatile memory element 108 coupled in parallel

with a transistor of one of the two inverters 104, 106. The inverters 104 and 106 include half-latch latch_0 and half-latch latch-1. So long as fg1 in the single nonvolatile memory element 108 is set near or below Gnd, pFET 108 will be turned on, and the output of inverter 104 will be pulled down to Gnd. Consequently, the latch will settle with Out = Gnd and OutBar = Vdd. If, however, fg1 is set well above Gnd, such that pFET 108 is turned off, the state to which the latch latches is not necessarily deterministic. To make the latching more deterministic, the gate width-to-length ratio of a pFET (or nFET, or both) of one of the two inverters 106, 108 can be adjusted so that the difference in transistor sizes beneficially disrupts the symmetry of the asymmetric latch when the nonvolatile memory element 108 is off, thereby influencing the fuse to latch deterministically with Out = Vdd and OutBar = Gnd.

Please amend paragraph **[0032]** *as follows:*

FIG. 11 shows how, as an alternative (or in addition) to adjusting transistor sizes, a capacitor 112 may be coupled to either the OutBar or Out terminals of the asymmetric fuses 94, 102 in FIGS. 9 and 10, respectively, to enhance deterministic latching, according to an embodiment of the present invention. Consider FIG. 11 as an example. Suppose for this example that floating-gate fg1 is programmed so that pFET 120 is conducting. Before a power-up or reset, the Out terminal is at Gnd potential and capacitor 112 is discharged. Because the capacitor 112 is initially uncharged, as Vdd is ramped up the Out terminal can only rise slowly, because capacitor 112 must be charged. Consequently, as Vdd ramps up OutBar will rise more rapidly, causing the cross-coupled inverters 114, ~~118~~ 116 of latch 118 to latch with OutBar high and Out low. Hence, the presence of the capacitor 112 aids the latch 118 to latch to a state with OutBar high and Out low.

Please amend paragraph **[0036]** *as follows:*

Referring now to FIGS. 12A, 12B, and 12C, there are shown rewriteable electronic logic-gate fuses 121, 122, and 127, according to embodiments of the present invention, in which a logic gate is combined with one or more nonvolatile memory elements, rather than combining a latch with one or more nonvolatile memory elements as described in the fuse embodiments above. In the generic logic-gate fuse embodiment shown in FIG. 12A, a logic gate 121 with n

fuse inputs (fg-0 – fg-n) and m data inputs (input-0 – input-m) implements an (n + m) input logic function. Those of ordinary skill in the art will readily understand that logic gate 121 can represent any of the standard logic function such as AND, OR, NAND, NOR, XOR, and XNOR, as well as complex combinations of these generic functions. In the particular embodiment shown in FIG. 12B, logic gate 122 is a CMOS inverter with n = 1 fuse inputs and m = 0 data inputs, comprised of first and second nonvolatile memory elements nFET 124 and pFET 126 as shown. Use of the nonvolatile memory elements 124, 126 ensures that the logic gate 122 settles to and provides a predetermined output following application of a power supply source to the logic gate 122. To ensure proper logic-gate operation and to avoid static power consumption, the memory value of the nonvolatile memory elements 124, 126 (e.g., the floating-gate fg0 voltage) should be maintained near or above Vdd or near or below ground, to ensure that one of nFET 124 or pFET 126 is conducting and the other one is not, as is standard practice in CMOS logic. In the particular embodiment shown in FIG. 12C, logic gate 127 is a 2-input CMOS NAND with n = 1 fuse inputs and m = 1 data inputs. The floating gate of the one of the devices therein is designated fg0. Those of ordinary skill in the art will recognize how to construct multi-input logic gates of varying type and complexity given the examples provided by this disclosure.

Please amend paragraph **[0042]** *as follows:*

Similar to the master-slave fuses 134, 136 in FIGS. 14 and 15, the master-slave logic-gate fuses 138, 140 in FIGS. 16 and 17 have a master signal terminal coupled to their respective master fuse. The master signal terminal is configured to receive a $\overline{\text{RESET}}$ power signal. The master-slave fuses 138, 140 in FIGS. 16 and 17 also include a slave latch 132, which is coupled to the master fuse 130, and is configured to receive a slave-latch signal (e.g., a $\overline{\text{RESET}}$ power signal) at its respective slave-latch terminal. The master fuse 130 in FIG. 17 provides first and second output signals latch_m0 and latch_m1 which are coupled to inputs of the slave latch 132 as shown.

Please amend paragraph **[0044]** *as follows:*

Referring now to FIG. 18, there is shown a rewriteable electronic fuse circuit 146 that includes a rewriteable electronic fuse 72 from FIG 7, and buffering circuits 150 and 152 coupled

to the fuse 72 outputs, in accordance with an embodiment of the present invention. The fuse 72 comprises a pair of cross-coupled CMOS inverters 74', 76', with the output latch_1 of inverter 74' being coupled to the input of inverter 76', and the output latch_0 of inverter 76' being coupled to the input of inverter 74'. The two non-volatile memory elements 78' and 80' have floating gates fg1 and fg0, respectively. The buffering circuits 150, 152 help prevent load-induced errors. For example, referring to fuse 72 in FIG. 7, a capacitive load on Out, such as might arise from another circuit connected to Out, could cause Out to rise more slowly than OutBar at power-up, and could cause fuse 72 to settle to an incorrect state. Buffering circuits 150, 152 in FIG. 18 isolate external loads from fuse 72, thereby helping to ensure that fuse 72 settles to the correct state at power-up. Buffering circuits 150, 152 likewise help prevent fuse 72 from being driven to an incorrect state by glitches on external load circuits connected to Out or Outbar. Whereas each fuse output in FIG 18 is shown to be double-buffered (two inverters connected in series), those of ordinary skill in the art will now readily understand that other types of buffering (e.g., single, triple, other gate types, etc.) may be used. Further, whereas fuse buffering is shown in FIG. 18 as being applied to symmetrical serial fuse (e.g., of the type shown in FIG. 7), the fuse buffering aspect of the present invention may also be used with other of the fuse types described in this disclosure.

Please amend paragraph **[0045]** *as follows:*

FIG. 19 shows a rewriteable electronic fuse 154 having an initialize circuit 156, according to an embodiment of the present invention. The fuse 154 includes non-volatile memory elements 153 and 155 having floating gates fg1 and fg0, respectively. The initialize circuit 156 includes first and second nFET switches 158 and 160, which have gates coupled to a an initialize signal terminal and sources coupled to Gnd. The drain of the first nFET switch 158 is coupled to a first latch terminal, latch_0, and the drain of the second nFET switch 160 is coupled to a second latch terminal, latch_1. Applying the initialize signal causes the initialize circuit 156 to drive latch terminals latch_0 and latch_1 to Gnd; releasing the initialize signal allows latch terminals latch_0 and latch_1 in fuse 154 to re-settle to a predetermined output. Initialize circuit 156 can be used (1) before power-up, to ensure that latch_0 and latch_1 are discharged prior to power-up; (2) during power-up, to hold latch_0 and latch_1 at ground until Vdd is stable and noise free; (3)

after power-up, to cause fuse 154 to reset if the power-up was noisy or had glitches; or (4) periodically, to ensure that fuse 154 reloads its data periodically and thereby corrects errors due to noise or cosmic particles that upset the latch state. Whereas the initialize circuit 156 in FIG. 19 is shown as being applied to a symmetrical serial fuse (e.g., of the type shown in FIG. 7 above), those of ordinary skill in the art will now readily appreciate and understand that the initialize circuit aspect of the present invention may also be used with other of the fuse types described in this disclosure. Likewise, those of ordinary skill in the art will readily appreciate and understand that any mechanism employed to initialize an electronic fuse, such as using pFETs rather than nFETs for the initializing transistors, or initializing latch_0 and latch_1 to Vdd rather than to Gnd, or temporarily shorting latch_0 and latch_1 together using transistors, or a range of other possibilities, is within the spirit and scope of this aspect of the present invention.

Please amend paragraph **[0046]** *as follows:*

As described above in relation to FIGS. 5A–5F, the nonvolatile memory elements used in the various fuse embodiments of the present invention may comprise floating-gate transistors. The amount of charge stored on the floating gate of such a floating-gate transistor determines the memory value (i.e. the floating-gate voltage) of the floating-gate transistor. Adding electrons to or removing electrons from the floating gate can modify this memory value. Accordingly, the predetermined state to which a fuse settles following a power-up or a reset of the fuse can be controlled and varied (i.e. can be written and rewritten) by adjusting the charge on the floating gate. One way of adjusting the charge resident on the floating gate of a floating-gate transistor is to connect a tunneling junction to the floating gate, and to tunnel electrons through the insulator that forms the tunneling junction using standard Fowler–Nordheim or direct-tunneling mechanisms. A tunneling junction can be implemented in various ways. For example, a MOSCAP tunneling junction may be formed using a MOS capacitor 162, as shown in FIG. 20. This tunneling junction includes V_tun conductor terminal and a floating gate. The junction is comprises p- substrate in which is formed an n- well having a n+ region coupled to the V_tun conductor terminal. As another example, the tunneling junction may be a pFET tunneling junction formed using a shorted pFET 164, as shown in FIG. 21. In this tunneling junction, n+ and p+ regions provided in an n- well disposed in a p- substrate are shorted together as shown,

including the V_tun conductor terminal. Indeed, any capacitor structure, irrespective of the device from which it is formed may be used, as those of ordinary skill in the art will now readily appreciate and understand.

Please amend paragraph **[0050]** *as follows:*

The bidirectional tunneling technique described above can be applied individually to any of the floating-gate memory elements used in any of the fuse embodiments described above. While individual application may be performed, more than one floating-gate memory element can, nevertheless, be programmed at the same time. FIG. 23 shows, for example, how two floating-gate voltages (i.e. memory values) of the floating-gate elements in a symmetric fuse may be modified at the same time. Note that only the floating-gate memory elements 174 and 178 of the symmetric fuse are shown in FIG. 23, it being understood that the remainder of the fuse is embodied as described in the manner above (e.g., see FIG. 7 above). According to this embodiment of the present invention, first and second floating-gate transistors 174 and 178 are coupled to respective first and second bidirectional tunneling control circuits 180 and 182 via floating gates 187 and 193, respectively. The first bidirectional tunneling control circuit 180 includes a small tunneling capacitor 184 and a large tunneling capacitor 186, in a manner similar to the bidirectional tunneling control circuit described in FIG. 22. The small tunneling capacitor 184 of the first bidirectional tunneling control circuit 180 has a first plate coupled to the floating gate fg0 187 of the first floating-gate transistor 174, and an opposing (i.e. second) plate coupled to a first high-voltage terminal, HV_fg0. The large tunneling capacitor 186 of the first bidirectional tunneling control circuit 180 has a first plate coupled to the floating gate fg0 187 of the first floating-gate transistor 174 and an opposing (i.e. second) plate coupled to a second high-voltage terminal, HV_fg1. The second bidirectional tunneling control circuit 182 also includes large and small tunneling capacitors 190 and 192. The small tunneling capacitor 192 of the second bidirectional tunneling control circuit 182 has a first plate coupled to the floating gate fg1 193 of the second floating-gate transistor 178, and an opposing (i.e. second) plate coupled to the second high-voltage terminal, HV_fg1. The large tunneling capacitor 190 of the second bidirectional tunneling control circuit 182 has a first plate coupled to the floating gate fg1 193 of the second floating-gate transistor 178 and an opposing (i.e. second) plate coupled to the first

high-voltage terminal, HV_fg0.

Please amend paragraph **[0051]** *as follows:*

Notice that the second plate of the small capacitor 184 in the first bidirectional tunneling control circuit 180 in FIG. 23 is coupled to the first high-voltage terminal, HV_fg0, but the second plate of the small capacitor 192 in the second bidirectional tunneling control circuit 182 is coupled to the second high-voltage terminal, HV_fg1. Also notice that the second plate of the large capacitor 186 in the first bidirectional tunneling control circuit 180 is coupled to the second high-voltage terminal, HV_fg1, but the second plate of the large capacitor 190 in the second bidirectional tunneling control circuit 182 is coupled to the first high-voltage terminal, HV_fg0. Applying the bidirectional tunneling technique described in relation to FIG. 22 to the tunneling junctions in FIG. 23 allows the floating gate 187 of the first floating-gate transistor 174 to be tunneled up, while at the same time the floating gate 193 of the second floating-gate transistor 178 to be tunneled down, or vice versa.

Please amend paragraph **[0055]** *as follows:*

FIG. 25 shows a block diagram of a bit cell 201 which combines a high-voltage switch (HVSW) such as that illustrated in FIG. 24 with the rewriteable electronic fuse of FIG 19. High-voltage switch HVSW has output HVout connected to the first high voltage terminal HV_fg0 of the fuse and output $\overline{HVout}$ connected the second high voltage terminal HV_fg1 of the fuse. Those of ordinary skill in the art will now realize that other combinations of switches and fuses could also be used as desired in response to the goals of the designer. Bit cell 201 has as inputs in the configuration shown, the logical input signals, Set and Reset, and Initialize; and the voltage signals Vdd, Gnd, High-Voltage and Intermediate-Voltage. Bit cell 201's outputs are Out (Ai) and $\overline{\text{Out}}$ (OutBar) ($\overline{Ai}$). In other configurations bit cell 201 may have more or fewer inputs and/or outputs as will now be apparent to those of ordinary skill in the art. Bit cell 201 is intended to be exemplary only to show how such cells may be arranged in the figures that follow and thus shouldn't be read to limit in any way the scope of the claims.

Please amend paragraph **[0057]** *as follows:*

Whereas FIG. 26 shows a plurality of bit cells (like bit cell 201 in FIG. 25) disposed in an array pattern, other embodiments of the present invention allow a plurality of bit cells to be distributed in an irregular but predetermined configuration (i.e. in a non-array configuration). FIG. 27 shows an exemplary embodiment of such a plurality of bit cells 250-1, 250-2,...,250-*n* (*n* is an integer greater than or equal to two), which are distributed in a possibly irregular but predetermined configuration. A shift register 252, comprised of a plurality of flip-flops (FF) 254-1, 254-2,...,254-*n*, is coupled to the plurality of bit cells 250-1, 250-2,...,250-*n* as shown. Programming bits are loaded into the shift register 252 via a data line (shown as DATA and $\overline{\text{DATA}}$ and labeled D and $\overline{D}$, respectively, in the figure) in response to a CLOCK signal applied to clock inputs of the flip-flops 254-1, 254-2,...,254-*n*. The outputs (Q, $\overline{\text{Q}}$) of the plurality of flip-flops 254-1, 254-2,...,254-*n* are coupled as shown to the plurality of bit cells 250-1, 250-2,...,250-*n*. After all programming bits have been shifted into the flip-flops 254-1, 254-2,...,254-*n* of the distributed shift register 252, a primary High-Voltage switch S1 (as well as an Intermediate-Voltage switch S2, and Vdd switch S3) is closed to connect a High-Voltage power supply, HV, to the high-voltage input terminals of the plurality of bit cells 250-1, 250-2,...,250-*n*. An initialize terminal is provided at S0. Application of the High-Voltage power supply to the high-voltage input terminals of the bit cells 250-1, 250-2, ..., 250-*n* causes the memory values (e.g., the floating-gate voltages of floating-gate transistors embedded in the bit cell) to be set to the programming values resulting in predictable outputs at $A_1, \overline{A_1}; A_2, \overline{A_2} \ldots A_n, \overline{A_n}$. Using a high voltage to modify the bit-cell memory values (i.e. the floating-gate voltages of the floating-gate transistors) was described in detail above (see, for example, the bidirectional tunneling discussion in connection with FIGS. 22 and 24). After the memory values have been set to a predetermined level, each of the plurality of fuses settles to a predetermined state following a power-up or reset of the fuse, in manner that has been described in detail above.

Please amend paragraph **[0058]** *as follows:*

FIG. 28 shows a rewriteable electronic fuse 260 incorporating many of the various aspects of the present invention described above. Although the fuse type shown is a symmetric

serial fuse as described above in connection with FIG. 7, other of the fuse types described above may alternatively be used in this embodiment. Each output of the latch is coupled to double-buffers 262 and 264. As described above in connection with FIG. 18, buffering the latch outputs helps to prevent load-induced bit errors. First and second capacitors 266 and 268 are also coupled to each of the latch outputs. As described above in connection with FIG. 11, the presence of one or both of the capacitors 266, 268 further assists in ensuring that the latch 270 having cross-coupled latch connections latch_0 and latch_1 latches to a predetermined state. The electronic fuse 260 also contains a reset circuit 272. As described above in connection with FIG. 19, the reset circuit 272 ensures that latch terminals latch_0 and latch_1 are reset to Gnd before latching ensues. Finally, the first and second nonvolatile memory elements 274 and 276, which in this example comprise floating-gate pFETs, have floating gates that are coupled to respective first and second bidirectional tunneling control circuits 278 and 280 which are in turn connected to first and second high voltage terminals HV_fg0 and HV_fg1, respectively. As described above in connection with FIGS. 22 and 23, the bidirectional tunneling control circuits 278, 280 permit the modification and control of the amount of charge stored on the floating gates of the first and second floating-gate transistors 274, 276. Further, as also described in detail above, the ability to control and modify the floating-gate voltages (i.e. the memory values) of the first and second floating-gate transistors 274, 276 allows the latch 270 of the fuse 260 to settle to a predetermined state following a power-up or a reset of the fuse 260.

Please amend paragraph **[0060]** *as follows:*

FIGS. 29A and 29B show a cross-sectional view (FIG. 29A) and a layout view (FIG. 29B) of a configuration comprising two p-type single-poly floating gate MOSFETs 300 similar to the one shown in FIG. 5A. This configuration, whose fabrication may use LOCOS (local oxidation of silicon) or STI (shallow trench isolation) technology as indicated, uses a combination of FN-tunneling and IHEI to remove electrons from or add electrons to the floating gate, thereby modifying the floating-gate charge. To remove electrons, a positive high voltage is applied between a first plate of the tunneling capacitor 302 and the floating gate 304, thereby inducing FN electron tunneling and causing electrons to tunnel off floating gate 304. The tunneling capacitor 302 includes an n- well formed in the p- substrate. To add electrons,

negatively biasing the drain 306 of the floating-gate MOSFET 300 by more than about 3V relative to the source 308 induces a large channel-to-drain electric field, causing holes to rapidly accelerate in MOSFET 300's channel-to-drain depletion region. MOSFET 300 includes an n-well formed in the p- substrate, with p+ regions corresponding to a source and drain being formed in the n- well. Some of the accelerated holes may collide with the semiconductor lattice and ionize electron-hole pairs. Some of the ionized electrons, as well as additional electrons generated by band-to-band electron tunneling in the same channel-to-drain depletion region, are expelled from the channel-to-drain depletion region by this same channel-to-drain electric field. If expelled with sufficient kinetic energy, some of these expelled electrons can be scattered upward and injected onto floating gate 304. These are depicted by the arrow designated electron injection. In the top plan view of FIG. 29B, there is shown a metal source, contact can and p+ source diffusion region of the source of MOSFET 300 and the p+ drain diffusion region. Also shown the n+ well contact well and p+ diffusion region of the short pFET 302.